REMARKS/ARGUMENTS

Reconsideration of the present application, as amended, is respectfully requested.

The January 23, 2006 Office Action and the Examiner's comments have been carefully considered. In response, claims are amended and remarks are set forth below in a sincere effort to place the present application in form for allowance. The amendments are supported by the application as originally filed. Therefore, no new matter is added.

Inasmuch as the present Amendment raises no new issues for consideration, and, in any event, places the present application in condition for allowance or in better condition for consideration on appeal, its entry under the provisions of 37 CFR 1.116 is respectfully requested.

PRIOR ART REJECTIONS

In the Office Action claims 1-3, 5-9, 11, 12 and 14-18 are rejected under 35 USC 103(a) as being unpatentable over USP 5,510,807 (Lee et al.) in view of USP 5,825,343 (Moon). Claims 10 and 19 are rejected under 35 USC 103 as being unpatentable over Lee et al. in view of Moon, and further in view of USP 6,825,823 (Taira et al.).

In response, claims 1 and 12 are amended to more clearly define the present claimed invention. Specifically, claim 1 is amended to include limitations from claim 2. Claim 12 is amended in a manner similar to the amendments to claim 1. The remaining claim amendments are made to maintain the consistent use of claim terminology.

The present claimed invention as defined by amended claim 1 is directed to a liquid crystal display device including a liquid crystal display panel having a plurality of signal lines, a plurality of scanning lines, a plurality of display pixels arrayed in a matrix and provided respectively near cross-points between the signal lines and the scanning lines through switching elements, and a driver which supplies the plurality of signal lines with a display signal in a field period, and which supplies the plurality of scanning lines with a scanning signal, to apply the display signal to the plurality of display pixels. The driver includes means which supplies an initialization signal including a constant single pulse voltage to the plurality of signal lines and supplies a first gate pulse as the scanning signal to the display pixels. After completion of the supply of the initialization signal voltage to the plurality of signal lines and the first gate pulse to the plurality of scanning lines, and after a predetermined hold time, the display signal is

supplied to the plurality of signal lines and a second gate pulse is supplied as the scanning signal to the plurality of scanning lines, thereby applying the display signal to the display pixel, at least one signal application period being set within the field period. The liquid crystal display panel includes a plurality of pixel electrodes arrayed in a matrix through the switching elements, common electrodes being opposed to the pixel electrodes, and liquid crystal being sandwiched between the pixel electrodes and the common electrodes. The hold time is set to a time equal to or longer than a voltage-write response time of the liquid crystal in the display pixels.

The present claimed invention as defined by amended claim 12 is directed to a drive control method for a liquid crystal display device which has a plurality of signal lines, a plurality of scanning lines, and a plurality of display pixels arrayed in a matrix and provided respectively near cross-points between the signal lines and the scanning lines through switching elements. The plurality of display pixels includes a plurality of pixel electrodes arrayed in a matrix through the switching elements, with common electrodes opposed to the pixel electrodes, and liquid crystal sandwiched between the pixel electrodes and the common electrodes. The plurality of signal lines are supplied with a display signal in a field period and scanning signals are

supplied to the plurality of scanning lines, to apply the display signal to the plurality of display pixels. The method includes the steps of providing at least one signal application period in the field period, applying an initialization signal including a constant single pulse to the display pixels, by supplying the initialization signal to the plurality of signal lines and supplying a first gate pulse as the scanning signal to the scanning lines. The method also includes applying the display signal to the display pixels by supplying the display signal to the plurality of signal lines and supplying a second gate pulse as the scanning signal to the plurality of scanning lines after a predetermined voltage hold time has passed after completion of applying the initialization signal to the display pixels and after completion of applying the first gate pulse to the plurality of scanning lines. The hold time is set to a time equal to or longer than a voltage-write response time of the crystal liquid in the display pixels.

Regarding the liquid crystal display apparatus and the drive control method thereof of amended claims 1 and 12, in at least one signal application period set within the field period, a first gate pulse is supplied to scanning lines, and after completion of the supply of the first gate pulse to the scanning lines and after a predetermined hold time, the second gate pulse

is supplied. An initialization signal is supplied to signal lines according to the timing of the supply of the first gate pulse, and a display signal is supplied to the signal lines according to the timing of the supply of the second gate pulse.

In the hold time after completion of the supply of the first gate pulse, the initialization signal is written in the liquid crystal in the display pixels, and the hold time is set to a time equal to or longer than a voltage-write response time of the liquid crystal in the display pixels. As a result, the initialization signal voltage is written in the liquid crystal in the display pixels by the time the hold time is completed.

When the display signal is supplied to the signal lines according to the timing of the supply of the second gate pulse, the liquid crystal does not respond immediately to the value of the supplied display signal, as the pulse width of the gate pulse is short.

Although the capacity of the liquid crystal varies depending on the written voltage value, the capacity of the liquid crystal immediately after the second gate pulse has been supplied is approximately a fixed value regardless of the display signal value, as the initialization signal is set at a fixed value.

The value of the voltage fluctuation (field through voltage) which occurs in the pixel electrode immediately after completion

of the supply of the gate pulse depends on the capacity value of the liquid crystal. However, as the capacity value of the liquid crystal is substantially fixed at the point immediately after completion of the supply of the second gate pulse, the voltage fluctuation amount of the pixel electrode immediately after completion of the supply of the gate pulse is fixed regardless of the value of the display signal.

As described above, as the value of the voltage fluctuation amount in the display pixel is substantially fixed, it is easy to cancel the voltage fluctuation amount by a value of the common electrode voltage, for example. Thus, the present invention has the advantage of obtaining a favorable display quality.

Lee at al. disclose a structure in which video data is sequentially applied for each block of a data line after a precharge pulse is applied to each data line during a period in which a scan signal is applied to a scan line.

As shown in Fig. 4 of Lee et al., odd numbered data lines are precharged to a positive V+ level, and even numbered data lines are precharged to a negative V- level. The V+ voltage level is close to the maximum voltage 5V and lower than 5V, and the V- voltage level is close to the minimum voltage OV and higher than OV. As shown in Fig. 6, the precharge time period is set to 6 μs, and the video data time period is set to 7 μs. The

data line and a pixel capacitor are charged to a precharge voltage V+/V- during the precharge time period of 6 μs, and to the maximum voltage 5V/minimum voltage OV during the video data time period of 7 μs.

The precharge pulse of Lee et al. is set to a reverse polarity (V+/V-) in even and odd numbered data lines. The present claimed invention is patentable over Lee et al. in that the initialization signal voltage is set to a fixed value with respect to the plurality of signal lines (see claim 1, lines 12-15; claim 12, lines 17-21).

In data lines of block #2 onward of Lee et al., a time interval is provided until video data is applied after the precharge pulse is applied. In Lee et al., a scan signal is applied to the scan line during the time interval. Thus, the time interval of Lee et al. is different from that of the present claimed invention in which a hold time is provided between the first and second gate pulses (see claim 1, lines 30-32; claim 12, lines 30-32).

Moon discloses a structure in which a gate pulse of a scan period (1H) is applied twice at a 1H interval with respect to one gate line, and the liquid crystal capacity Clc is precharged by a first gate pulse.

However, as shown in Fig. 8 of Moon, the interval of the two gate pulses with respect to one gate line is structured so as to match the application period of the gate pulse with respect to the other gate line. The time interval of the present claimed invention is different from Moon in that the hold time is set to a time equal to or longer than a voltage-write response time of the liquid crystal in the display pixels.

Even when combining Lee et al. with Moon, Lee et al. and Moon do not disclose a structure for applying two gate pulses to a scan line at a time interval equal to or longer than a voltage-write response time of the liquid crystal in the display pixels. Thus, Lee et al. and Moon do not disclose, teach or suggest the invention as defined by amended claims 1 and 12.

In view of all of the foregoing, claims 1 and 12 are patentable over the cited references under 35 USC 102 as well as 35 USC 103.

Claims 2, 3, 5-11 and 14-19 are either directly or indirectly dependent on claims 1 or 12. The dependent claims are patentable over the cited references in view of their dependence on claims 1 or 12, and because the references do not disclose, teach or suggest each of limitations set forth in the dependent claims.

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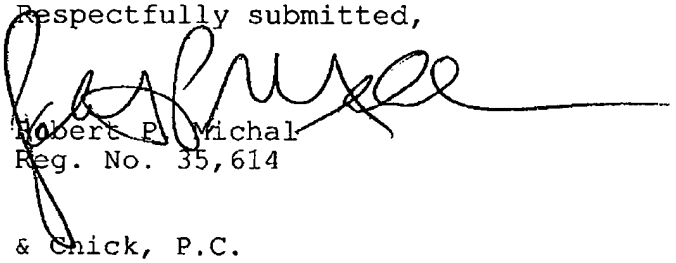
Entry of this Amendment under the provisions of 37 CFR 1.116, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner disagrees with any of the foregoing, the Examiner is respectfully requested to point out where there is support for a contrary view.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,



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